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DESIGN OF ASYNCHRONOUS VITERBI DECODER USING DUAL-RAIL PROTOCOL FOR LOW POWER CONSUMPTION

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Abstract: -

Paper shows the review of asynchronous Viterbi decoder using hand shake protocol as Dual – Rail protocol. Viterbi decoders are used for decoding convolution forward error correction codes in a large proportion of digital transmission systems including mobile phones and digital television. For portable applications, the battery size and lifetime is of commercial importance as is the size of the electronics. The approach adopted in the Viterbi design is to use a self-timed (or asynchronous) timing strategy. This saves power through not having to generate or distribute a global clock. Instead, timing between blocks is performed by local handshake signals. This enables an asynchronous system to only consume power when doing useful work and to have an idle power of near zero. Furthermore, there is an inherent advantage to asynchronous systems in that a system can switch almost instantaneously between the idle state and maximum activity; this is much more difficult to organize in a clocking system.

Keywords: - *Viterbi Algorithm, Synchronous, Asynchronous, Handshake Protocol (Dual Rail Protocol).*

1 INTRODUCTION

Due to the recent trend towards multi-gigahertz systems, there are increasing design challenges to managing clock distribution. Asynchronous design, which replaces global clocking with local handshaking, has the potential to make low power consumption design more feasible. Moreover, the use of local handshaking, instead of global clocking, imparts the ability of localized flow control to the asynchronous pipeline. Dual-rail is a commonly-used scheme to implement an asynchronous data path. In dual-rail, two wires (or rails) are used to implement each bit. The wires indicate both the value of the bit, and also its validity. In terms of power consumption, synchronous systems involve higher switching activity than asynchronous ones. High switching activity translates into a large amount of wasted power. On the other hand, in data driven asynchronous systems, idle parts consume negligible power and switching activity is associated only with useful work being done: a valuable feature for battery operated systems. Asynchronous systems produce less electromagnetic emissions than their synchronous counterparts which generate spurious signals at the operating clock frequency and its entire harmonics. These signals interfere with cellular phones, television and navigation systems. Synchronous or asynchronous design options can be considered in the implementation of the Viterbi decoder.

Viterbi Decoder

Viterbi decoders are widely used in digital transmission and recording systems and are expected to be used in next generation wireless applications. Such portable, battery operated systems, require low-power consumption as well as high processing speeds, over 100 Mb/s, to allow multimedia transmission.

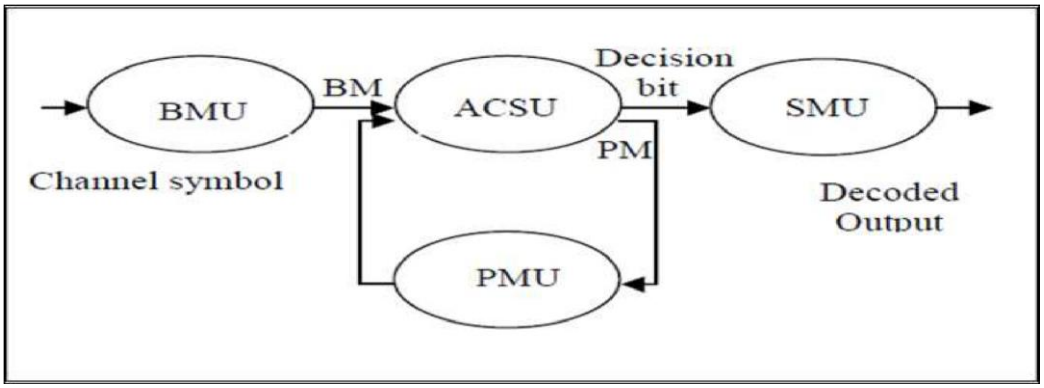

Fig:1 shows a block diagram of Viterbi Decoder

BRANCH METRIC UNIT (BMU): - This unit computes the branch metric of each transition, which is a hamming distance between the received symbol and expected symbol. The architecture of the BMU comprises of a XOR gate and a counter.

ADD COMPARE SELECT UNIT (ACSU): - The ACS unit is used to calculate the path metrics for each state in current stage from path metrics of its two previous states and the associated state-transition branch metric, and then the path with least path metric is selected as survival path for the state in current stage.

PATH METRIC UNIT (PMU): - It computes the partial path metrics at each node in the trellis.

SURVIVOR MANAGEMENT UNIT (SMU): - This is responsible for keeping track of the information bits associated with the surviving paths designated by the path metric Calculation.

I. Synchronous vs. Asynchronous

There are many serial data transfer protocols. For serial data transfer the protocols can be grouped into two types: Asynchronous and Synchronous:-

For synchronous data transfer, both the receiver and sender access the data according to the same clock. Therefore, a special line for the clock signal is required. A master should provide the clock signal to all the receivers in the synchronous data transfer. For asynchronous data transfer, there is no common clock signal between the sender and receivers. Therefore, on a data transfer speed the sender and the receiver first need to agree. This speed usually does not change after the data transfer begins. Both the sender and receiver set up their own internal circuits to make sure that the data accessing is follows that agreement. However, computer clocks also differ in accuracy just like some watches run faster than others,. Although the difference is very small, it can accumulate fast and finally cause errors in data transfer. This mix-up is solved by adding synchronization bits at the front, middle or end of the data. Since the synchronization is done frequently, the receiver can correct the clock gathering error. The synchronization information may be added to to every frame of data or every byte of data. Sending these extra synchronization bits slows down the actual data transfer rate and may account for up to 50% data transfer overhead.

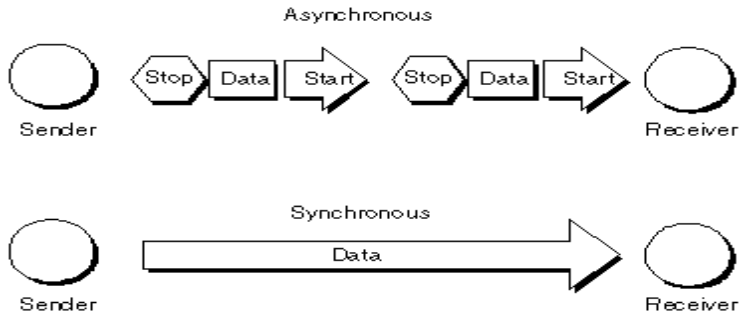

Fig:2 shows the comparison diagram of Asynchronous vs. Synchronous

II. Asynchronous Viterbi Decoder

Asynchronous circuits are composed of blocks that communicate to each other by handshaking via asynchronous channels, in order to carry out the required synchronization, communication, and sequencing of operations. Asynchronous communication channel consists of a bundle of and a protocol to communicate the data between the blocks. It has two types of encoding scheme in asynchronous channels. If the encoding scheme uses one wire per bit to transmit the data and a request line to identify when the data is valid is called single-rail encoding. The channel is called a bundled-data channel. Alternatively, in dual-rail encoding the data is sent using two wires for each bit of information. Dual rail Encoding allows for data validity to be indicated by the data itself.

III.Convolution Encoder

An encoder is a Mealy machine, where the output is a function of the current state and the current input. It consists of multiple XOR gates and one or more shift registers. The stream of information bits flows in to the shift register from one end and is shifted out at the other end. Some stages are connected to XOR gates of the shift registers as well as to the current input to generate the output.

IV.HANDSHAKE PROTOCOL AS DUAL RAIL

Protocol

Dual-rail is a commonly-used intrigue to implement an asynchronous data path. In dual-rail, two wires (or rails) are used to implement each bit. The wires indicate both the value of the bit, and also its validity. In the 4-phase implementation, encodings of 01 and 10 correspond to valid data values 0 and 1, respectively. The encoding 00 indicates the reset or spacer state with no valid data and 11 is an unused (i.e., illegal) encoding. Encodings on the data path typically alternate between valid values and the reset state. Since the data path itself indicates the viability of each bit, dual-rail is effective in designing asynchronous data paths which are highly robust in the presence of arbitrary delays. Unlike in the 4-phase implementation, where definite codes represent definite values, in 2-phase, a new data is marked by a transition in the corresponding bit. A transition in false/true line indicates a zero/one respectively.

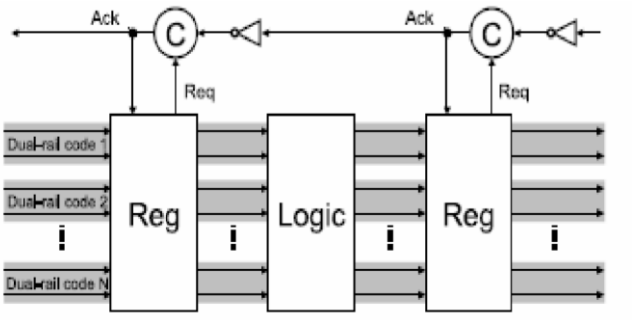

Fig: 3 Pipelining of Dual-Rail Protocol

V. Conclusion

A Survey on Viterbi Decoder shows, Viterbi Decoder is the most power-hungry module in the system. So Asynchronous techniques like Dual-Rail protocol is used as a handshaking protocol to make Viterbi decoder asynchronous are using VHDL. The approach adopted in the Viterbi design is to use a self-timed (or asynchronous) timing strategy. This saves wer through not having to generate or distribute a global Clock. An asynchronous system to only consume power when doing useful work and to have an idle power of near zero.

VI.References

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